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**PLASMA ENHANCED CHEMICAL VAPOR
DEPOSITION METHODS AND SEMICONDUCTOR
PROCESSING METHODS OF FORMING LAYERS
AND SHALLOW TRENCH ISOLATION REGIONS**

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1 PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION METHODS
2 AND SEMICONDUCTOR PROCESSING METHODS OF FORMING
3 LAYERS AND SHALLOW TRENCH ISOLATION REGIONS

4 TECHNICAL FIELD

5 This invention relates to plasma enhanced chemical vapor
6 deposition methods, to semiconductor processing methods of forming
7 layers and shallow trench isolation regions, and to plasma enhanced
8 chemical vapor deposition methods of forming SiO₂ comprising layers.

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10 BACKGROUND OF THE INVENTION

11 The processing of a semiconductor substrate to form integrated
12 circuitry involves forming numerous layers over the substrate. Many of
13 the layers are formed by a chemical vapor deposition (CVD) process
14 involving placing the substrate within an elevated temperature
15 environment provided by a reactor and providing reactant gases within
16 the reactor. Successive layers are provided by successive CVD processes.
17 However, characteristic temperatures of a typical CVD process may not
18 be conducive to layers already formed over the substrate. For example,
19 subsequent CVD processing of a substrate having an aluminum layer will
20 cause unacceptable alloying of the aluminum into the substrate.
21 Accordingly, plasma enhanced chemical vapor deposition (PECVD)
22 techniques were developed that include forming a plasma within a reactor
23 and using the energy of the plasma in an environment with a lower

1 temperature to form the layers. Consequently, the PECVD process is
2 more conducive to temperature sensitive layers than a non-plasma CVD
3 process.

4 PECVD systems typically feature a parallel plate chamber within
5 a reactor operated at a low pressure. A plasma source is used to
6 generate a plasma field within the reactor, for example, radio-frequency-
7 induced glow discharge, high density inductively coupled plasma, or other
8 plasma sources within an environment of reactant gases provided within
9 the reactor. Such PECVD systems are physically similar to plasma etch
10 systems, and therefore, are capable of using the plasma field for etching
11 a semiconductor substrate layer during the deposition processing.

12 One CVD and/or PECVD process forms shallow trench isolation
13 regions within a substrate. A substrate having trench openings formed
14 therein is provided within a reactor to form layers over the trenches
15 thereby filling the same. However, as the semiconductor industry strives
16 to increase the density of components per unit area of semiconductor
17 substrate, the width of the trench openings continues to shrink such that
18 depositing the layer within the trenches can be problematic.

19 Figs. 1-2 illustrate the problem. A semiconductor substrate is
20 generally indicated by numeral 10 and comprises a bulk substrate 12
21 having trenches 14 formed therein. The substrate is provided in a
22 reactor (not shown) and a layer of insulative material 16 is deposited
23 over the substrate 12 within the trenches 14. As layer 16 is deposited,

1 the insulative material begins to build up over corners 17 of the
2 trenches 14 forming facets or bread-loafing regions 18.

3 Referring to Fig. 2, as layer 16 continues to be deposited, the
4 bread-loafing regions 18 begin to occlude the trench openings and form
5 voids 20 within the portion of layer 16 that progresses into the
6 trenches 14. These voids 20 can be detrimental to the performance of
7 the isolation regions.

8 To overcome this problem, inductively coupled plasma reactors can
9 be used with a bias being placed upon the substrate during deposition.
10 The bias attracts ions in the plasma to bombard the layer 16 effectively
11 producing a simultaneous deposition to sputter etching aspect of
12 processing layer 16. The purpose and result of the sputter etching is
13 to remove the bread-loafing regions 18 during deposition of layer 16, i.e.,
14 forming the bread-loafing regions 18, removing at least some of the
15 bread-loafing regions 18, forming the bread-loafing regions 18 and
16 continuing the process until the trenches 14 are filled. The deposition
17 to sputter etching aspect establishes a deposition to sputter etching ratio
18 (also referred to as deposition to etch ratio and/or D:S ratio). An
19 exemplary D/S ratio comprises a constant 6:1. This process can improve
20 the deposition of layer 16 within the trenches 14.

21 However, such processing is not without its own drawbacks. Fig. 3
22 illustrates a problem (like numerals from the previously described
23 embodiment are employed where appropriate with the difference being

1 indicated with a suffix (b) or with different numerals). Consider corner
2 sections 17 of substrate 12. The etching portion of the processing can
3 cause corner sections 17 to be etched away from substrate 12 thereby
4 changing the profile of trenches 14. Changing the profile of trenches 14
5 can detrimentally affect the performance of the isolation regions.
6 Additionally, removed material from corners 17, designated with
7 numeral 24, can settle within the trenches 14 inside layer 16. Since the
8 removed material 24 is routinely not an insulative material as is
9 characteristically used for isolation regions, the performance of the
10 isolation regions is typically detrimentally affected.

11 12 SUMMARY OF THE INVENTION

13 In accordance with an aspect of the invention, a substrate is
14 placed within a plasma enhanced chemical vapor deposition reactor. A
15 plurality of reactant gases are provided within the reactor proximate the
16 substrate under high density plasma conditions effective to form a layer
17 on the substrate. The conditions result in etching portions of the layer
18 during its formation and thereby include a deposition to etch ratio of
19 forming the layer. During the forming, the conditions are changed to
20 change the deposition to etch ratio.

21 In another aspect of the invention, the invention includes a
22 semiconductor processing method of forming shallow trench isolation
23 regions within a semiconductive substrate. Isolation trenches are formed

1 within the semiconductive substrate. The substrate is provided within a
2 plasma enhanced chemical vapor deposition reactor. A silane containing
3 gas, an oxygen containing gas and an inert gas are injected into the
4 reactor under high density plasma conditions effective to form a
5 predominate SiO₂ comprising layer on the substrate to overfill the
6 trenches. The conditions result in etching of portions of the layer
7 during its formation and thereby includes a deposition to etch ratio of
8 the forming SiO₂ comprising layer. During the forming, the conditions
9 are changed to change the deposition to etch ratio.

10 In yet another aspect of the invention, a substrate is placed within
11 a plasma enhanced chemical vapor deposition reactor. A plurality of
12 reactant gases are provided within the reactor proximate the substrate
13 under plasma conditions. The plasma conditions are effective to form
14 a substantially homogeneous layer of material on the substrate. While
15 continuing to form the layer, a flow of at least one of the reactant
16 gases is reduced during at least some of the forming.

17 BRIEF DESCRIPTION OF THE DRAWINGS

18 Preferred embodiments of the invention are described below with
19 reference to the following accompanying drawings.

20 Fig. 1 is a first embodiment of a fragmentary sectional view of a
21 prior art semiconductor substrate discussed in the "background" section
22 above.
23

1 Fig. 2 is a view of the Fig. 1 substrate fragment at a processing
2 step subsequent to that shown in Fig. 1.

3 Fig. 3 is a second embodiment of a fragmentary sectional view of
4 a prior art semiconductor substrate discussed in the "background" section
5 above.

6 Fig. 4 is a fragmentary sectional view of a semiconductor substrate
7 at one processing step in accordance with an embodiment of the
8 invention.

9 Fig. 5 is a view of the Fig. 4 substrate fragment at a processing
10 step subsequent to that shown in Fig. 4.

11 Fig. 6 is a view of the Fig. 4 substrate fragment at a processing
12 step subsequent to that shown in Fig. 5.

13 Fig. 7 is a graphical representation of an aspect of the processing
14 in accordance with one embodiment of the invention.

15 Fig. 8 is a graphical representation of an aspect of the processing
16 in accordance with one embodiment of the invention.

17
18 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

19 This disclosure of the invention is submitted in furtherance of the
20 constitutional purposes of the U.S. Patent Laws "to promote the progress
21 of science and useful arts" (Article 1, Section 8).

22 To aid in interpretation of the claims that follow, the terms
23 "semiconductive substrate" and "semiconductor substrate" are defined to

1 mean any construction comprising semiconductive material, including, but
2 not limited to, bulk semiconductive materials such as a semiconductive
3 wafer (either alone or in assemblies comprising other materials thereon),
4 and semiconductive material layers (either alone or in assemblies
5 comprising other materials). The term "substrate" refers to any
6 supporting structure, including, but not limited to, the semiconductive
7 substrates described above.

8 With reference to Figs. 4-7, an embodiment of the method of the
9 present invention is illustrated. This embodiment encompasses a
10 semiconductor processing method, particularly a plasma enhanced chemical
11 vapor deposition method of forming shallow trench isolation regions
12 within a semiconductor substrate. Referring to Fig. 4, a semiconductor
13 substrate 42 in process is indicated generally by reference numeral 40.
14 An exemplary semiconductor substrate 42 comprises bulk substrate
15 material, for example, monocrystalline silicon. Isolation trenches 44 are
16 formed within the semiconductor substrate 42 by etching methods known
17 in the industry, and include corners 48. The substrate 42 is provided
18 within a plasma enhanced chemical vapor deposition reactor (not shown).
19 An exemplary reactor comprises an inductively coupled plasma reactor
20 capable of producing a high density plasma. In the context of this
21 document, "high density" refers to a plasma having at least 10^9 ions/cm³
22 plasma density.
23

1 A plurality of reactant gases are provided within the reactor
2 proximate the substrate 42 under plasma conditions, most preferably high
3 density plasma conditions, effective to form a layer 46 on the
4 substrate 42 and within trenches 44. An exemplary layer 46 comprises
5 an electrically insulative material, for example, silicon dioxide. Exemplary
6 reactant gases comprise a silane containing gas, an oxygen containing gas
7 and an inert gas, for example, argon. An exemplary environment within
8 the reactor includes a pressure preferably ranging from 0.1 mTorr to 50
9 mTorr, more preferably less than 5 mTorr, and a temperature of
10 about 650°C. Exemplary flow rates of the reactant gases into the
11 reactor comprise ranges of: argon at 0-300 sccm, oxygen at 100-300
12 sccm and silane at 20-200 sccm. The preferred high density plasma
13 conditions result in etching of portions of the layer 46 during its
14 formation and thereby include a deposition to etch ratio of the forming
15 layer 46. An exemplary preferred initial D/S ratio of forming layer 46
16 is at least 7:1. This high deposition rate relative to the sputter etching
17 rate is intended to keep outer corners 48 of the trenches covered by
18 enough of forming layer 46 to protect such corners from being removed
19 from the sputter etching action.

20 Referring to Fig. 5, deposition continues with the high density
21 plasma conditions being changed during the forming to change the
22 deposition to etch ratio. Most preferably, the deposition to etch ratio
23 is decreased. Regardless, processing preferably continues to completely

1 fill trenches 44, as shown in Fig. 6. Preferably, layer 46 as formed is
2 substantially homogeneous throughout.

3 Changing of the conditions during the forming to change the
4 deposition to etch ratio might occur by a number of manners. Such
5 manners might include maintaining some parameters constant while
6 changing one or more other parameters or changing a plurality of the
7 operating parameters during the formation regardless. By way of
8 example only, changing of the conditions might comprise changing a flow
9 rate of at least one reactant gas to the reactor during formation, and/or
10 changing at least one power setting during formation such as bias power
11 on the substrate. Further, the changing conditions might comprise
12 maintaining constant power settings while changing a flow rate of at
13 least one reactant gas into the reactor during formation.

14 In one aspect, the invention contemplates providing conditions
15 which begin with an environment providing a large deposition rate
16 relative to an etch rate, thereafter decreasing the ratio, and thereafter
17 increasing the ratio. Such provides but one example where the changing
18 of the conditions reduces the deposition to etch ratio at least once
19 during formation. Preferably, the deposition starts with substantially no
20 etching during initial formation.

21 In one aspect of the invention, the invention contemplates changing
22 the conditions during the forming to continuously vary the deposition to
23 etch ratio throughout at least a majority of the forming. In one

1 preferred implementation, changing the condition comprises continuously
2 increasing the deposition to etch ratio at some point after a majority of
3 the layer has been formed.

4 In the trench-filling example of forming SiO_2 under high density
5 plasma conditions using a silane containing gas, an oxygen containing gas,
6 and an inert gas, one aspect of the invention contemplates reducing a
7 flow of at least one of the silane containing gas and the oxygen
8 containing gas, or both, during the forming and continuing forming the
9 layer. Such preferably has the effect of decreasing the deposition to
10 etch ratio until such time as one or more of the flows might be
11 increased. For example where the reactant gas silane is varied in such
12 example, an exemplary high flow rate would be from about 60 sccm to
13 about 150 sccm, with an exemplary low flow rate for silane being from
14 about 20 sccm to about 60 sccm.

15 Figs. 7-8 together graphically represent but one example
16 embodiment of the present invention where silane flow is varied during
17 formation. The process begins with an environment providing a large
18 silane flow rate which corresponds, referring to Fig. 8, to providing a
19 large deposition rate relative an etch rate. The deposition can start with
20 substantially no etching of the layer during its initial formation. After
21 this beginning, the silane flow rate is decreased which corresponds to
22 decreasing the ratio. (i.e., at some point in time after the deposition
23 begins, the etching increases relative to the deposition.) At some point

1 in the example, the silane flow is increased, corresponding to an increase
2 in the ratio, perhaps to a point which substantially eliminates etching
3 while continuing the deposition. The illustrated example depicts a
4 substantially continuous and parabolic profile, although any other profile
5 is contemplated, such as by way of example, linearly, exponentially and
6 logarithmically.

7 The invention was initially motivated and considered in the context
8 of high density plasma deposition involving an etching aspect during the
9 depositing. However, the invention also contemplates plasma enhanced
10 chemical vapor depositing by placing a substrate within a plasma
11 enhanced chemical vapor deposition reactor which may or may not be
12 a high density plasma reactor, and may or may not be operated under
13 high density plasma conditions. A plurality of reactant gases are then
14 provided within the reactor proximate the substrate under plasma
15 conditions effective to form a substantially homogeneous layer of material
16 on the substrate. At some point in the process, a flow of at least one
17 of the reactant gases is reduced during at least some of the forming and
18 the layer is continued to be formed.

19 In compliance with the statute, the invention has been described
20 in language more or less specific as to structural and methodical
21 features. It is to be understood, however, that the invention is not
22 limited to the specific features shown and described, since the means
23 herein disclosed comprise preferred forms of putting the invention into

1 effect. The invention is, therefore, claimed in any of its forms or
2 modifications within the proper scope of the appended claims
3 appropriately interpreted in accordance with the doctrine of equivalents.
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